Job Title: SR. DESIGN VERIFICATION ENGINEER

Employment Type: Full Time

Location: Hybrid/Mountain View, CA

Department: VLSI

Description:

We are looking for enthusiastic engineers to join the CPU/IP/SoC verification team. Working closely with the local design team, you will be responsible for verifying subsystems such as caches, memories, and interconnects, as well as their integration into the larger SoC. We are looking for highly talented, self-motivated, and versatile engineers that will push hardware to the highest performance and quality standards.

Responsibilities

- Own, develop, and drive the full verification process of SoC functional blocks
- Create verification content including test plans, test bench components, directed and constrained random tests, and functional coverage
- Broader responsibilities may include supporting full-chip simulation, emulation, and post-silicon bring-up

Qualifications

- Ability to clearly communicate across teams with multidisciplinary backgrounds
- BS or MS in EE
- 3+ years of experience in CPU, IP, or SoC verification
- Knowledge of high-level verification flow methodology (test plan development, constrained random test generation and debug, coverage analysis and closure)
- Experience with a class-based testbench using SystemVerilog or similar language
- Experience with UVM/OVM is required
- Experience with C/C++ and assembly is a plus
- Experience with Python, Perl, or other scripting languages is a plus
- Knowledge of memory coherence, DDR, AXI/ACE is a plus

Benefits

- Base salary range is $100,000 - $300,000
- The actual salary of a successful applicant may vary from the posted range based on a candidate’s experience, training, education, location, and/or other legitimate business reasons
- You will also be eligible for stock options and benefits